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Docket No. BUR920030118US1 (IBU-10-5799)

Applicant(s): Gill et al

Serial No.	**Filing Date**	**Examiner**	**Group Art Unit**
10/708,023	February 3, 2004	Kevin Quinto	2826

Invention:

STRUCTURE AND METHOD FOR LOCAL RESISTOR ELEMENT IN INTEGRATED CIRCUIT TECHNOLOGY

I hereby certify that this Response to Notice of Non-Compliant Amendment (37 CFR 1.121) is being transmitted via facsimile to the United States Patent and Trademark Office

Fax. No. 571-273-8300 on NOVEMBER 3, 2005 *(Date)* 22 *(No. of pages)*

TO: Legal Instruments Examiner Sherry Davis

Attached is a Response to Notice of Non-Compliant Amendment including the claim amendment sheets being filed in response to the notice issued on October 26, 2005 in connection with the subject application.

It is not believed that any fees are required. However, the Commissioner is hereby authorized to charge payment of fees associated with this communication, or credit any overpayment, to Deposit Account No. 09-0456.

FROM: Patrick J. Daugherty
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(Typed or Printed Name of Person Signing Certificate)

Carole Giacomazzo *(Signature)*

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Gill et al	)	Examiner: Kevin Quinto
Serial No. 10/708,023	)	Art Unit: 2826
Filed: February 3, 2004	)	Confirmation No. 2022
For: **STRUCTURE AND METHOD FOR LOCAL RESISTOR ELEMENT IN INTEGRATED CIRCUIT TECHNOLOGY**	)	

Attorney Docket No.: BUR920030118US1 (IBU-10-5799)

RESPONSE TO NOTICE OF NON-COMPLIANT AMENDMENT (37 CFR 1.121)

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Attention: Sherry Davis
Legal Instruments Examiner (LIE)

Dear Sir:

Responsive to the Notice of Non-Compliant Amendment issued October 26, 2005, applicants are re-submitting the claim amendments section to replace the version which accompanied the amendment of October 21, 2005, together with an explanation of the amendments made to claims 4 and 7.

AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Canceled)

3. (Currently amended) A method of forming a static random access memory device contact stud with an integral resistor, said method comprising the steps of:

a. providing a substrate having at least one contact area;

b. forming an insulating layer over said substrate, said insulating layer overlying and in contact with the contact area;

c. forming a contact hole in said insulating layer to expose the contact area;

d. providing a first conductive material into the contact hole to form a contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area; and

e. forming the integral resistor by disposing a thin resistive ~~material~~ film layer within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface;

wherein said integral resistor is in a circuit series connection with said contact stud between the contact area and an electrical node of said static random access memory device, the thin resistive film ~~material~~ layer located in a cross coupling between an M1 metal cross coupling node and a polysilicon gate node at either a contact-to-MI interface or a contact-to-polysilicon gate interface;

further comprising the step of limiting a width of the thin resistive film ~~material~~ layer to a width of the contact hole.

4. (Currently amended) A method of forming a bipolar transistor contact stud with an integral resistor, said method comprising the steps of:

a. providing a substrate having at least one contact area;

b. forming an insulating layer over said substrate, said insulating layer overlying and in contact with the contact area;

c. forming a contact hole in said insulating layer to expose the contact area;

d. providing a first conductive material into the contact hole to form a contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area; and

e. forming the integral resistor by disposing a resistive material layer within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface;

wherein said integral resistor is in a circuit series connection with said contact stud between the contact area and an electrical node of said bipolar transistor, the integral resistor has a resistance value of between about one Ohm and about ten Ohms, and the integral resistor is in circuit series connection with said contact stud with a base, emitter or collector of the bipolar transistor.

5. (Original) The method of claim 4, wherein the bipolar transistor is a silicon-on-insulator lateral diode, and the integral resistor and contact stud form a local resistor element in at least one of an anode, a cathode or a gate.

6. (Original) The method of claim 4, further comprising the step of placing a gate structure in parallel circuit connections to the local resistor element.

7. (Currently amended) A method of forming an integral resistor and contact stud within a contact hole within a semiconductor transistor drain structure, said method comprising the steps of:

a. providing a substrate having at least one contact area;

b. forming an insulating layer over said substrate, said insulating layer overlying and in contact with the contact area;

c. forming a contact hole in said insulating layer to expose the contact area;

d. providing a first conductive material into the contact hole to form a contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area;

e. forming the integral resistor by disposing a resistive material layer within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface;

f. placing the integral resistor and contact stud in a circuit series connection with a gate, the resistor having a resistance value of between about one Ohm and about ten Ohms, wherein the drain has a composite resistance not equal to a source composite

resistance and said integral resistor is in a circuit series connection with said contact stud between the contact area and an electrical node of said semiconductor[[:]].

8. (Original) The method of claim 7 wherein the device is a MOSFET and the integral resistor and contact stud form a first local resistor, further comprising the steps of:

forming a second integral resistor and contact stud within a contact hole within a gate, the second integral resistor having a resistance greater than about 10 Ohms;

placing the second integral resistor and second contact stud in a circuit series connection with the first local resistor.

9. (Original) The method of claim 8, further comprising the step of coupling the gate to ground through the second integral resistor.

10. (Previously presented) The method of claim 7, wherein the device is a MOSFET, further comprising the step of modulating current flow through the MOSFET by selective placement of a plurality of integral resistor and contact stud structures throughout the drain.

11. (Original) The method of claim 10 wherein the step of modulating current flow comprises the step of forming a plurality of contacts on a drain side of the MOSFET;

wherein the step of forming the integral resistor and contact stud comprises forming an integral resistor and a contact stud structure within each of a group of the plurality of contacts in an interdigitated pattern, the pattern comprising an alternating distribution of contacts and integral resistor and contact stud structures.

12. (Previously presented) A method of forming a SiGe transistor contact stud with an integral resistor, said method comprising the steps of:

a. providing a substrate having at least one contact area;

b. forming an insulating layer over said substrate, said insulating layer overlying and in contact with the contact area;

c. forming a contact hole in a base region or above an emitter in said insulating layer to expose the contact area;

d. providing a first conductive material into the contact hole to form a contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area; and

e. forming the integral resistor by disposing a resistive material layer within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface;

wherein said integral resistor is in a circuit series connection with said contact stud between the contact area and an electrical node of said SiGe transistor, and

modulating current flow through the transistor by selective placement of a plurality of the integral resistor and contact stud structures throughout the base region or